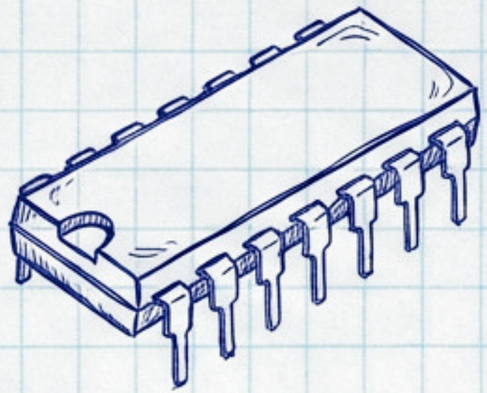
Notes By ~ Kamal Kishor

Digital Electronics & Computer Organization

(BCA-204) – Compiled Study Notes & Exam Solutions

- [x] Unit I: Number Systems & Logic Gates
- [x] Unit II: Boolean Algebra & Arithmetic Circuits
- [x] Unit III: Flip-Flops & Shift Registers
- [x] Unit IV: Counters & Memory



Strictly based on class notes & past papers (May 2018, 2019).

Unit 1: Decimal to Base-X Conversions

Method: Divide number by base, record remainder.

Decimal to Binary $(25)_{10}$ → (?)

2	25	
2	12	--- rem 1
2	6	--- rem 0
2	3	--- rem 0
2	1	--- rem 1
	0	--- rem 1

Read Bottom to Up

Result: $(11001)_2$

Decimal to Octal $(80)_{10}$ → (?)

8	80	
8	10	--- rem 0
8	1	--- rem 2
	0	--- rem 1

Result: $(120)_8$

Decimal to Hex $(57)_{10}$ → (?)

16	57	
16	3	--- rem 9
	0	--- rem 3

Result: $(39)_{16}$

Fractional Part $(0.125)_{10}$ → Binary

0.125 x 2 = 0.25 → bit 0
0.25 x 2 = 0.5 → bit 0
0.5 x 2 = 1.0 → bit 1

Result: $(0.001)_2$

Base-X to Decimal & Inter-Conversions

Formula: Sum of Weights (Digit x Base^Power)

Binary to Decimal: $(1001)_2 = 1*2^3 + 0 + 0 + 1*2^0 = 8 + 1 = 9$

Octal to Decimal: $(65)_8 = 6*8^1 + 5*8^0 = 48 + 5 = 53$

Hex to Decimal: $(FF)_{16} = 15*16^1 + 15*16^0 = 240 + 15 = 255$

Base-7 to Decimal: $(56)_7 = 5*7^1 + 6*7^0 = 35 + 6 = 41$

Shortcuts (Grouping)

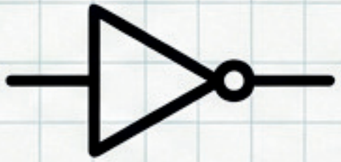
1 0 0 0 1 0 1

1 0 5

$(105)_8$

✳ Octal = 3 bits.
Hex = 4 bits.

Unit 1: Logic Gates – The Building Blocks

Name	Symbol	Truth Table	Expression
AND		A B | Y ✓ ✓ | ✗ 0 1 | ✗ 1 0 | ✗ 1 ✓ | ✗	Y = A.B
OR		A B | Y 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1	Y = A+B
NOT		A | Y 0 | 1 1 | 0	Y = A’
NAND		A B | Y 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0	Y = (AB)’
XOR		A B | Y 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0	Y = A (+) B

Universal Gates = NAND & NOR (Can build anything with just these!)

Unit II: Boolean Algebra Laws

Basic Rules:

$A + 0 = A$

$A \cdot 1 = A$

$A + A' = 1$

$A \cdot A' = 0$

Commutative: $A + B = B + A$

Distributive: $A(B+C) = AB + AC$

DeMorgan's Laws (Very Important!)

1. $(AB)' = A' + B'$ (Bubbled OR)
2. $(A+B)' = A' \cdot B'$ (Bubbled NAND)

Shannon Reduction (Decomposition):

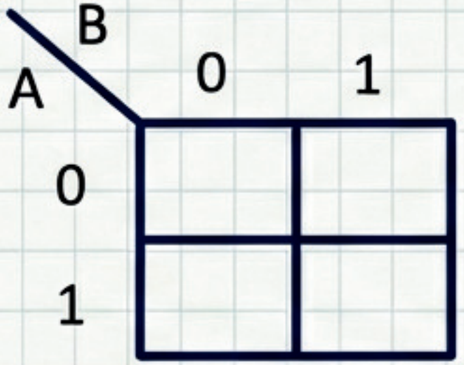
$F(A,B...) = A'.F(0,B...) + A.F(1,B...)$

Consensus Law: Redundancy Theorem

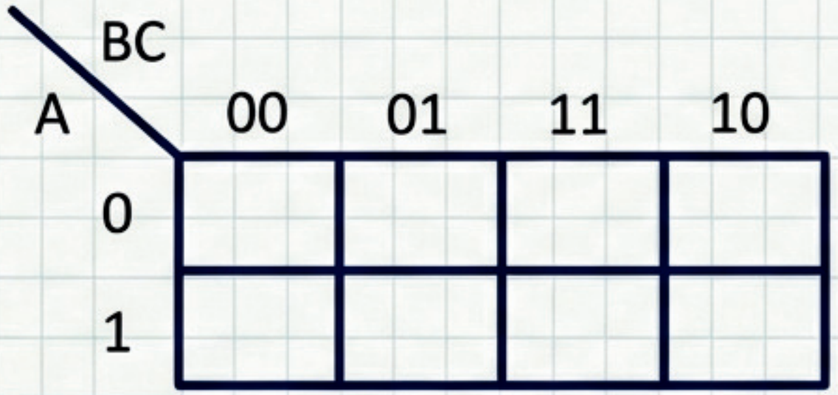
Karnaugh Maps (K-Maps)

Visual Simplification Method

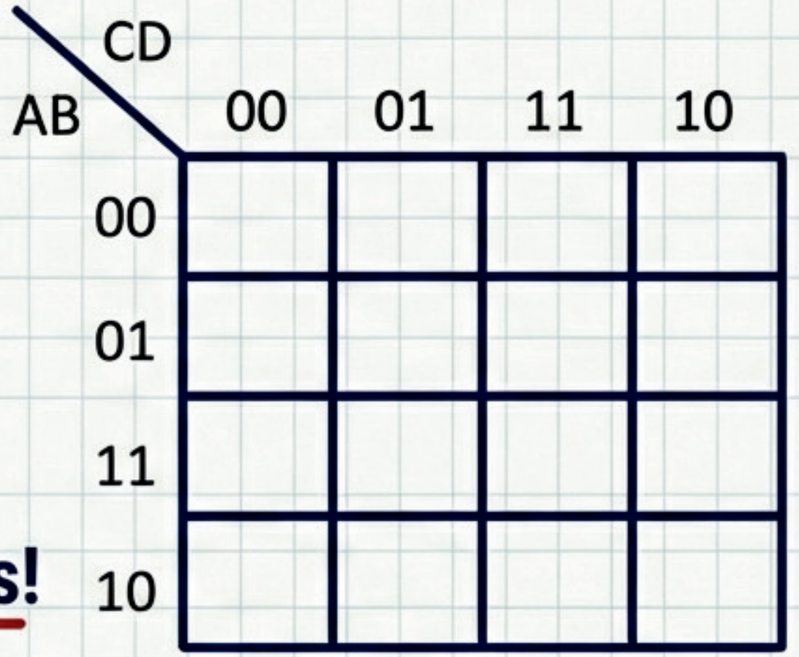
2-Variable



3-Variable



4-Variable

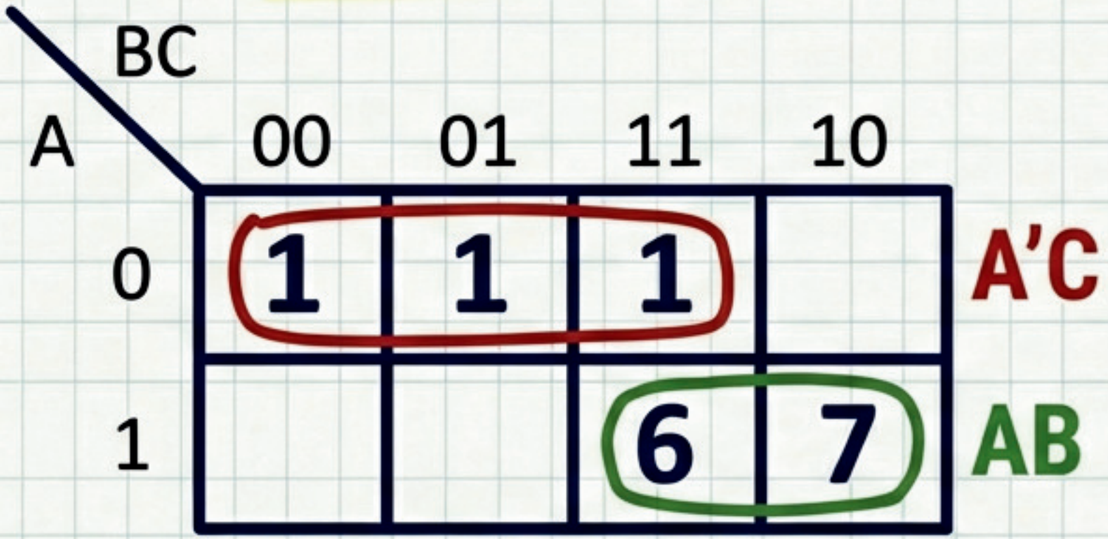


- **Rules**
  - Use Gray Code (00, 01, 11, 10) - Only 1 bit changes!
  - Group sizes: 1, 2, 4, 8, 16 (Powers of 2)
  - No Diagonals allowed.
  - Groups can Wrap Around.

Solving K-Maps: SOP vs. POS

SOP (Sum of Products)

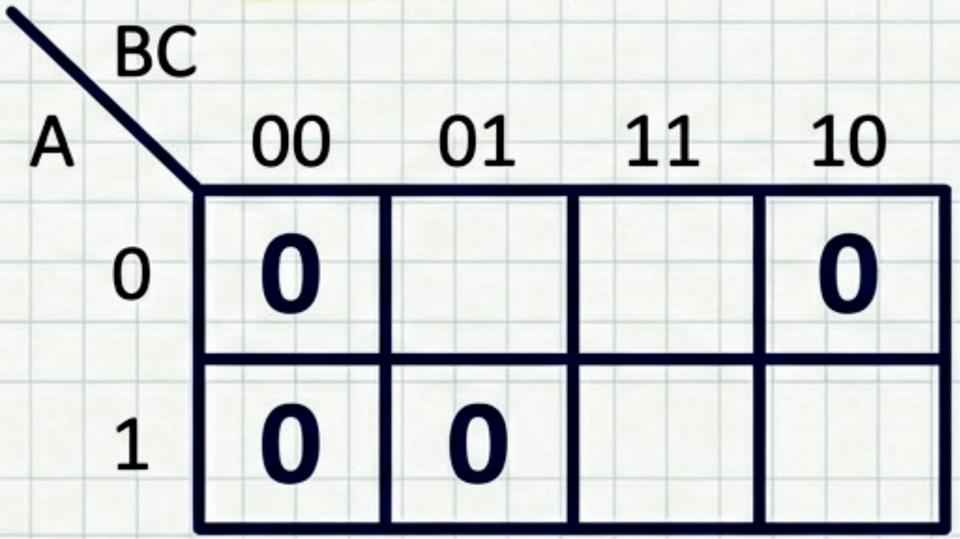
Group the 1s.



$$Z = A'C + AB$$

POS (Product of Sums)

Group the 0s.



$$(A+B)(A'+C)\ldots$$

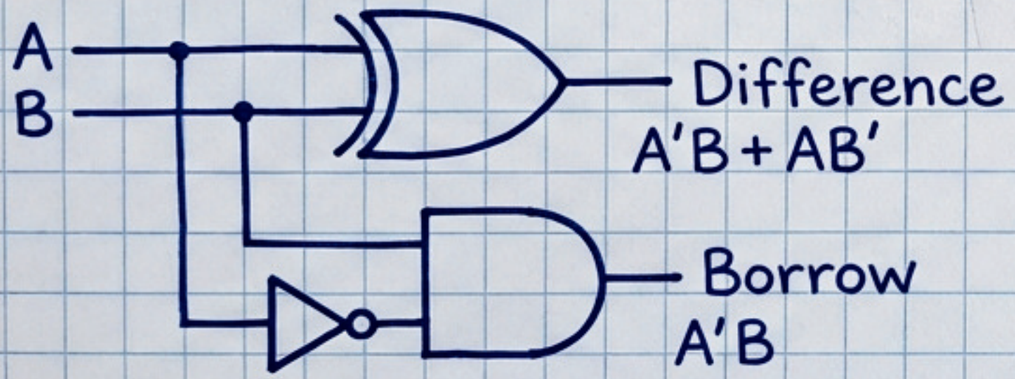
Minterm (m): 1 = A. **Maxterm (M): 0 = A.**

Arithmetic Circuits

Half Adder

Sum = A XOR B
Carry = A.B

Half Subtractor



Diff = A XOR B
Borrow = A'.B

Full Adder (3 bits)

Sum = A XOR B XOR Cin
Carry = AB + BCin + ACin

Made of 2 Half Adders + 1 OR Gate

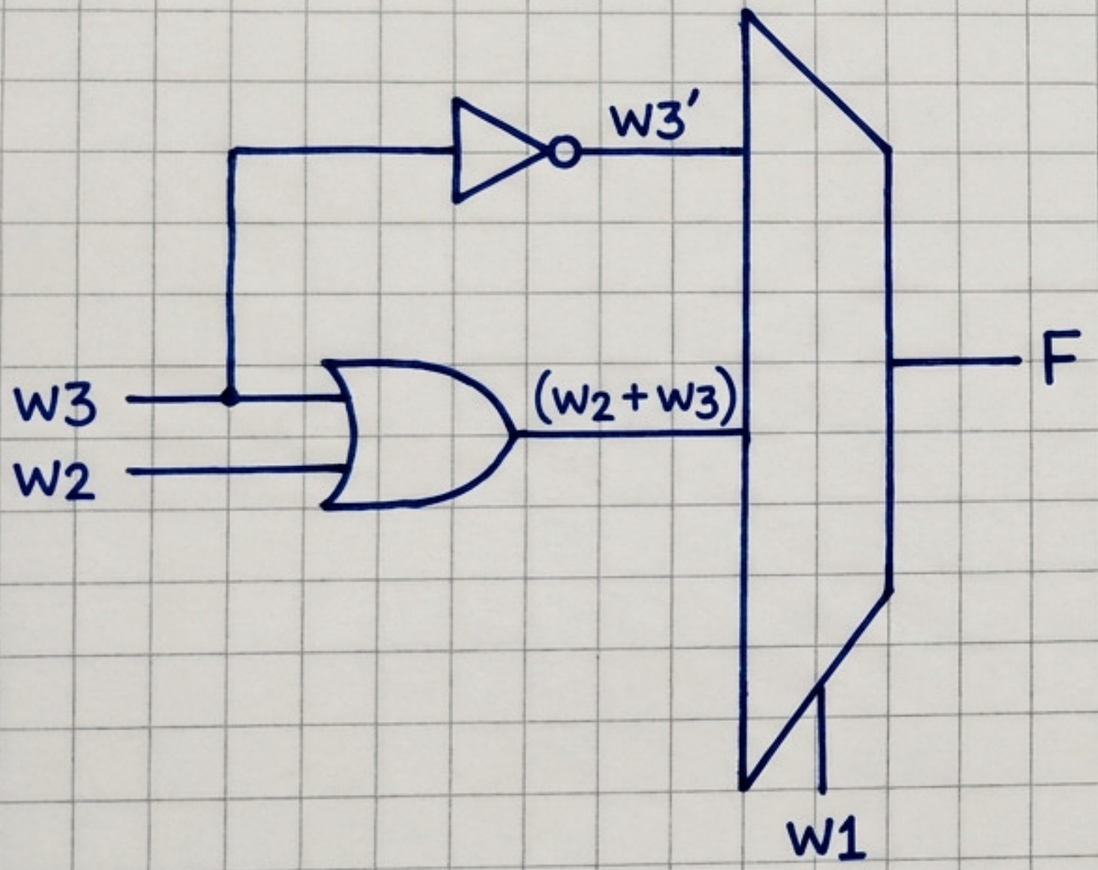
Full Subtractor

Diff = A XOR B XOR C
Borrow = A'B + A'(B XOR C) + BC

Data Handling Circuits

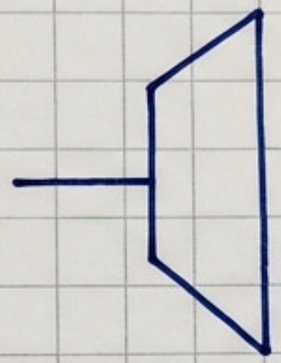
Multiplexer (MUX)

Many Inputs → 1 Output



Demultiplexer (DeMUX)

1 Input → Many Outputs

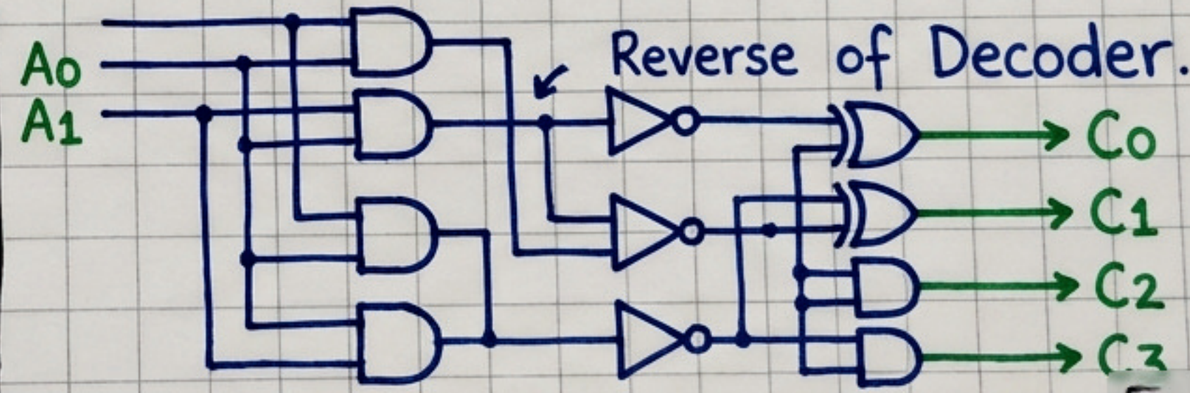


Decoder & Encoder

Decoder **Encoder**

n inputs → 2^n unique outputs

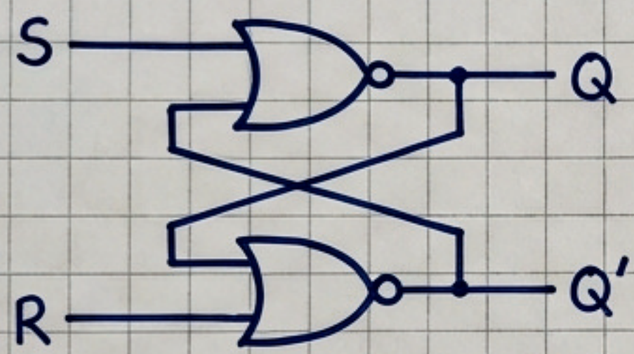
Ex: 3-to-8 Decoder



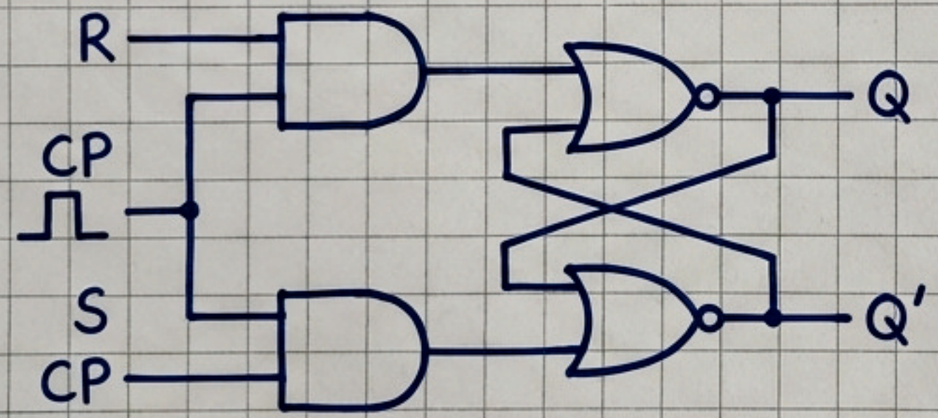
Unit III: Sequential Logic & Latches

Combinational = Present Input only.

Sequential = Present Input + Past Output (Memory).



S=0, R=0 → No Change
S=1, R=0 → Set (1)
S=0, R=1 → Reset (0)
S=1, R=1 → INVALID



Clocked SR Flip-Flop.

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Flip-Flops: JK, D, T & Master-Slave

JK Flip-Flop

Fixes the SR invalid state.

- If J=1, K=1 → Toggle State (Q becomes Q').

Race Around Condition

Problem in JK FF: If Clock is too long, output toggles uncontrollably.

Solution: Master-Slave JK Flip-Flop.

D Flip-Flop (Data/Delay)

Single input. Q(next) = D.

Used for storage.

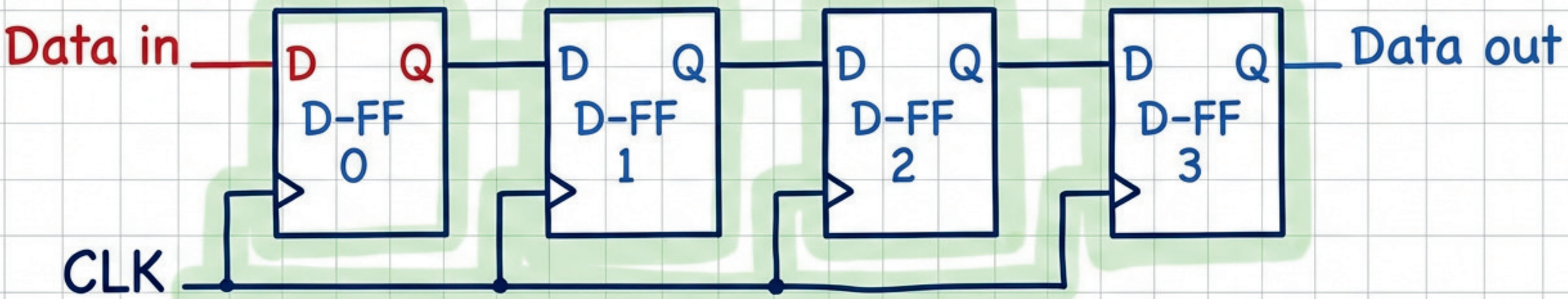
T Flip-Flop (Toggle)

Connect J & K together.

Excitation Table Summary		
D:	0→0 (0) 1→0 (0)	0→1 (1) 1→1 (1)

Shift Registers

Data Storage & Movement



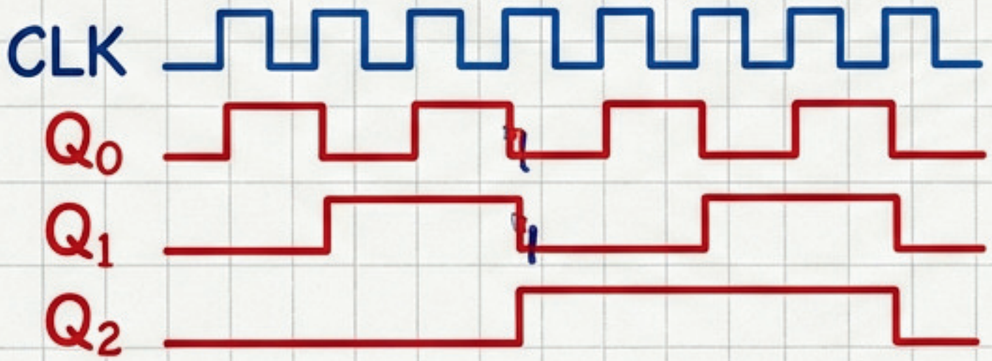
1. SISO (Serial In Serial Out) - Slowest
2. SIPO (Serial In Parallel Out)
3. PISO (Parallel In Serial Out)
4. PIPO (Parallel In Parallel Out) - Fastest

Bi-Directional Register can shift Left or Right.

Unit IV: Counters

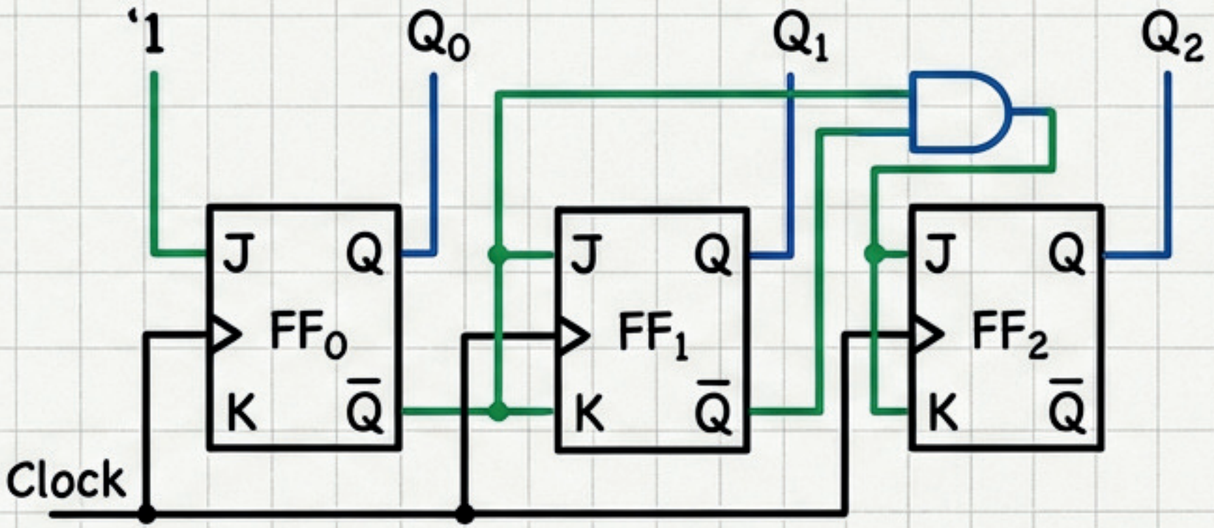
Asynchronous (Ripple) Counter

- Output of FF 1 is the Clock for FF 2.
- Pros: Simple.
- Cons: Slow (Delay).



Synchronous Counter

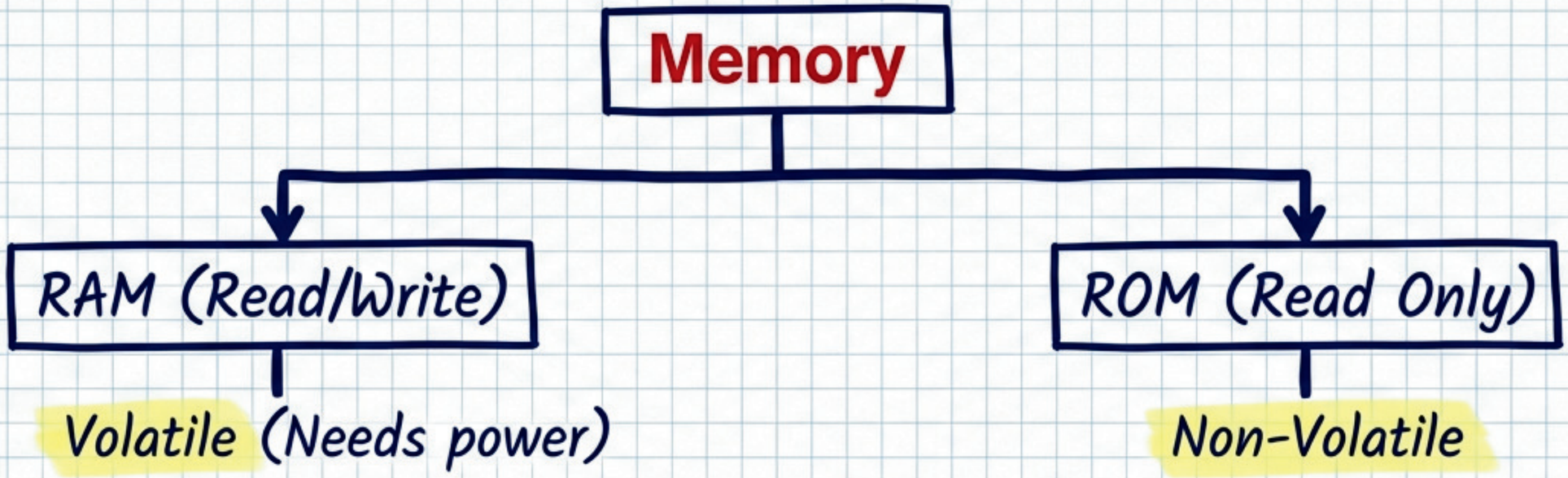
- All FFs clocked simultaneously.
- Faster operation.



Terms:

- Modulus (Mod): Number of states (e.g., Mod-10).
- Ring Counter: Feedback loop.
- Johnson Counter: Twisted Ring.

Memory Organization



- SRAM (Static): Flip-Flops, Fast, Cache.
- DRAM (Dynamic): Capacitors, Slow, Needs Refresh, Main Memory.

- PROM (Programmable)
- EPROM (Erasable UV)
- EEPROM (Electric Erasable)

Cache Memory = Small, high-speed bridge between CPU and RAM.

Important Exam Questions (Past Papers)

Question 1: Explain how 3 to 8 decoder function can be obtained from a demultiplexer.
(Cite: [Pasted from <IMAGE 0>])

Question 2: Simplify Boolean function:
F(ABCD) = Sum(0,2,3,6,7) + Don't Care(8,10,11,15).
(Cite: [Pasted from <IMAGE 1>])

Question 3: What is race around condition? Construct master slave flip-flop.
(Cite: [Pasted from <IMAGE 1>])

Question 4: Give the truth table and symbol for X-OR logic gate.
(Cite: [Pasted from <IMAGE 2>])

Question 5: Implement a full-subtractor with two half-subtractors and an OR-gate.
(Cite: [Pasted from <IMAGE 3>])

Practice these for the final!

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